

## 50 Gb/s D-FF

### Features

- Maximum data rate: 50 Gb/s
- Output amplitude: 0.9 V<sub>pp</sub>
- Single-ended clock/data input



### General Description

The CI0085B is a dynamic D-type Flip Flop (D-FF) operating at data rates up to 50 Gb/s. The I/O levels are SCFL (V<sub>H</sub>: 0.0 V, V<sub>L</sub>: -0.9 V). The IC is fabricated using a 0.1- $\mu$ m InP HEMT process. The CI0085B is provided in a hermetically-sealed package with V-connectors.

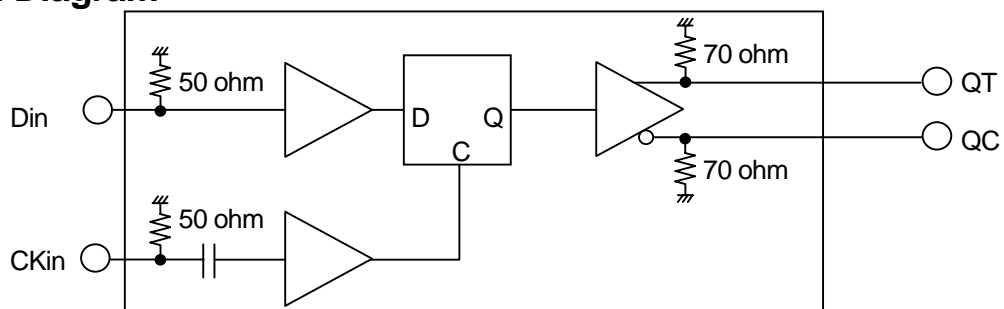
### Applications

- Waveform Shaping
- Data Retiming
- Decision Circuit

### Truth Table

Din	CKin	QT	QC
L		L	H
H		H	L
Otherwise No Change			

### Functional Diagram



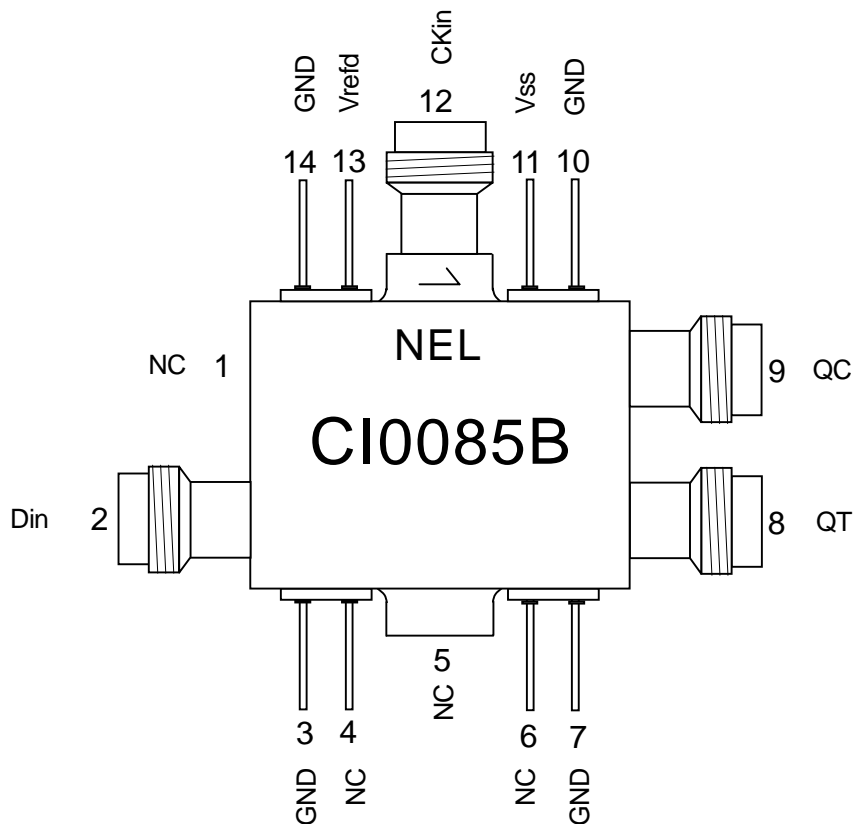
## Connection Table

No.	NAME	FUNCTION	No.	NAME	FUNCTION
1	NC	No Internal Connection	8	QT <sup>(1)</sup>	Data Output (True)
2	Din	Data Input	9	QC <sup>(1)</sup>	Data Output (Complementary)
3	GND	Ground (0.0 V)	10	GND	Ground (0.0 V)
4	NC	No Internal Connection	11	Vss	Power Supply (-4.5 V)
5	NC	No Internal Connection	12	CKin	Clock Input
6	NC	No Internal Connection	13	Vrefd <sup>(2)</sup>	Data Input Reference
7	GND	Ground (0.0 V)	14	GND	Ground (0.0 V)

### Notes

- (1) Terminate unused output connectors to GND through 50-ohm resistors.
- (2) Internally generated reference voltage that determines the data input threshold level. By Applying - 0.75V to - 0.2V externally to this pin an arbitrary threshold voltage can be established.

## Connection Diagram (Top View)



## Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
VSS	Power Supply Voltage	-5.0 to +0.1	V
Vin	Applied Voltage Amplitude at Clock Input (CKin)	1.2	V <sub>pp</sub>
Vind	Applied Voltage at Data Input (Din)	-1.2 to +0.1	V
Vinck	Applied Voltage at Clock Input (CKin)	-1.2 to +1.2	V
Vout	Applied Voltage at Data Outputs (QT, QC)	-1.5 to +0.2	V
Vrefd	Applied Voltage at Vrefd pin	-1.2 to +0.1	V
Tstor	Storage Temperature	TBD	°C
Tc <sup>(1)</sup>	Case Temperature under Bias	TBD	°C

TBD: To Be Determined

## Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VSS	Power Supply	-4.7	-4.5	-4.3	V
Vrefd	Data Input Reference Voltage	Open or adjust in the range from -0.75 V to -0.2 V			
Din	Data Input Interface	DC coupling (see DC Characteristics)			
CKin	Clock Input Interface	DC coupling (see DC Characteristics) or AC coupling (see AC Characteristics)			
QT,QC	Data Output Interface	DC coupling (see DC Characteristics) , Terminate to GND through 50 ohm			

## DC Characteristics

(V<sub>SS</sub> = -4.5 V, GND = 0.0 V, Tc<sup>(1)</sup> = 30 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
ISS	Power Supply Current		330	TBD	mA
VOH	Output Voltage, High (QT, QC)	TBD	0.0		V
VOL	Output Voltage, Low (QT, QC)		-0.9	TBD	V
VIH	Input Voltage, High (Din, CKin)	TBD	0.0		V
VIL	Input Voltage, Low (Din, CKin)		-0.9	TBD	V

TBD: To Be Determined

Note

(1) Tc: Temperature at package base.

## AC Characteristics (50 Gb/s)

(V<sub>SS</sub> = -4.5 V, GND = 0.0 V, PN = 31, MR = 1/2, V<sub>refd</sub>: Adjust in the range from -0.75 V to -0.2 V)

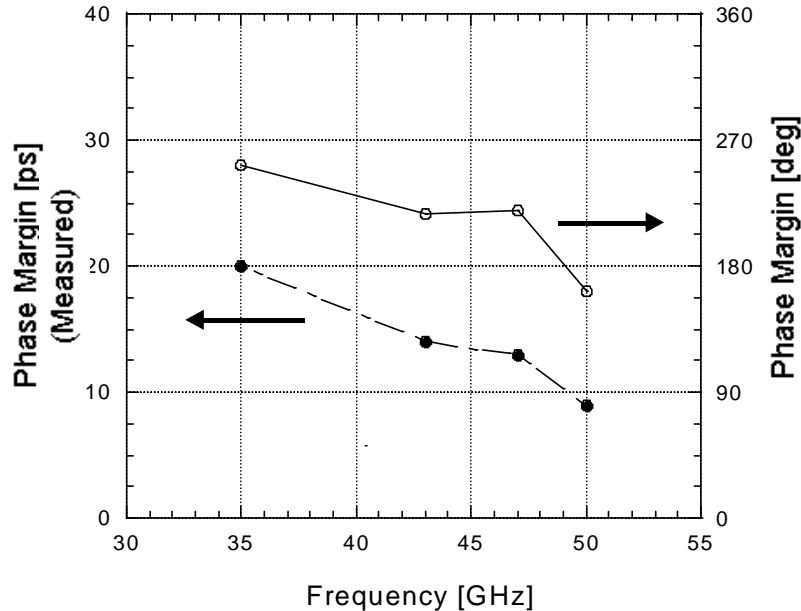
SYMBOL	PARAMETER	T <sub>c</sub> =30 °C			UNIT
		MIN.	TYP.	MAX.	
V <sub>in</sub>	Clock Input Voltage Amplitude	TBD	0.9		V <sub>pp</sub>
V <sub>center</sub>	Clock Input Center Voltage	-0.5		0.5	V
f <sub>MAX</sub>	Maximum Clock Frequency	50			GHz (1)
f <sub>MIN</sub>	Minimum Clock Frequency		35		GHz
V <sub>amp</sub>	Output Voltage Amplitude (QT, QC)	TBD	0.9		V <sub>pp</sub>
t <sub>r</sub>	Output Rise Time (QT, QC) 20 - 80%		10	TBD	ps
t <sub>f</sub>	Output Fall Time (QT, QC) 20 - 80%		10	TBD	ps
PM	Phase Margin		160		deg. (1), (2)

TBD: To Be Determined

### Notes

(1) Confirmed by error-free operation using pseudo-random pattern with a word length of 2<sup>31</sup>-1 bits at 50 Gb/s

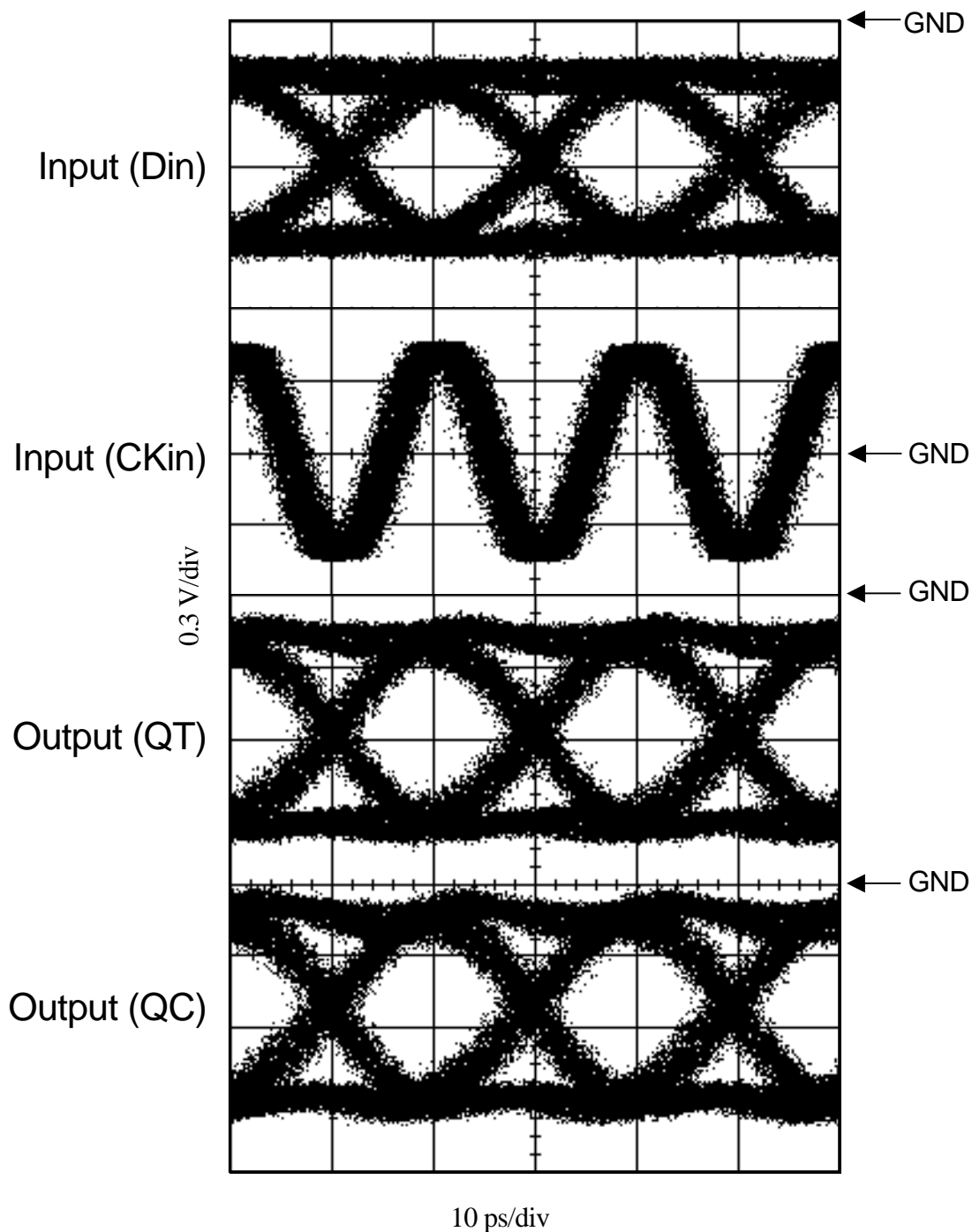
(2) Calculated as follows:  $PM [deg.] = \frac{PM (measured) [ps]}{1UI [ps]} \times 360 [deg.]$   
 where,  $1UI = \frac{1}{f}$  f: Clock frequency



### Measurement Conditions

V<sub>SS</sub> = -4.5 V, V<sub>refd</sub>: Optimum, Input Data: SCFL, Input Clock: 0.7 V<sub>pp</sub>

### Sample Waveforms (50 Gb/s)

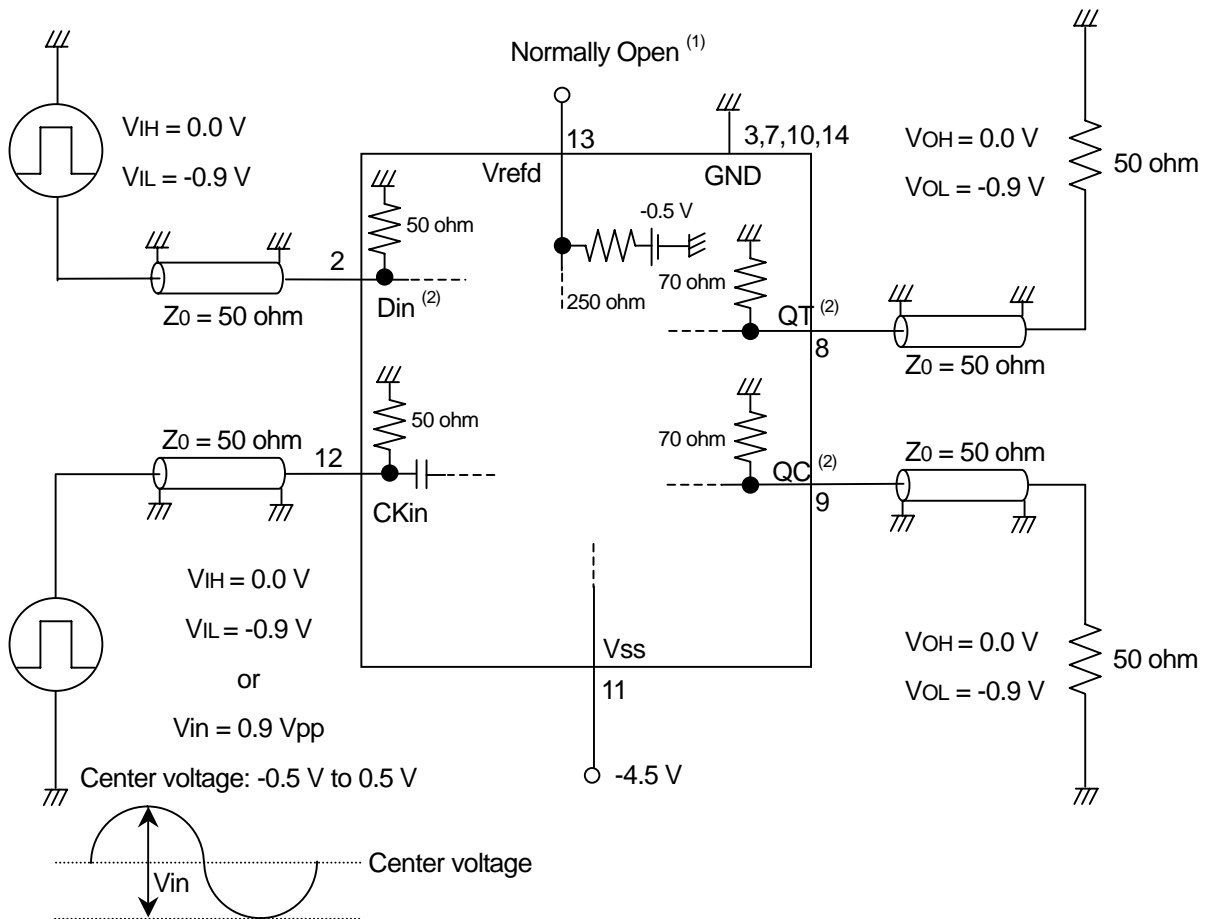


### Measurement Conditions

$V_{ss} = -4.5 \text{ V}$ ,  $V_{refd}$  : Optimum, Input Data: 50 Gb/s, Input Clock: 50 GHz

## Sample Implementation

Note: Each number corresponds to a pin or a connector as shown in Connection Diagram



### Note

- (1) Open or adjust in the range from  $-0.75\text{ V}$  to  $-0.2\text{ V}$ .
- (2) DC coupling only.

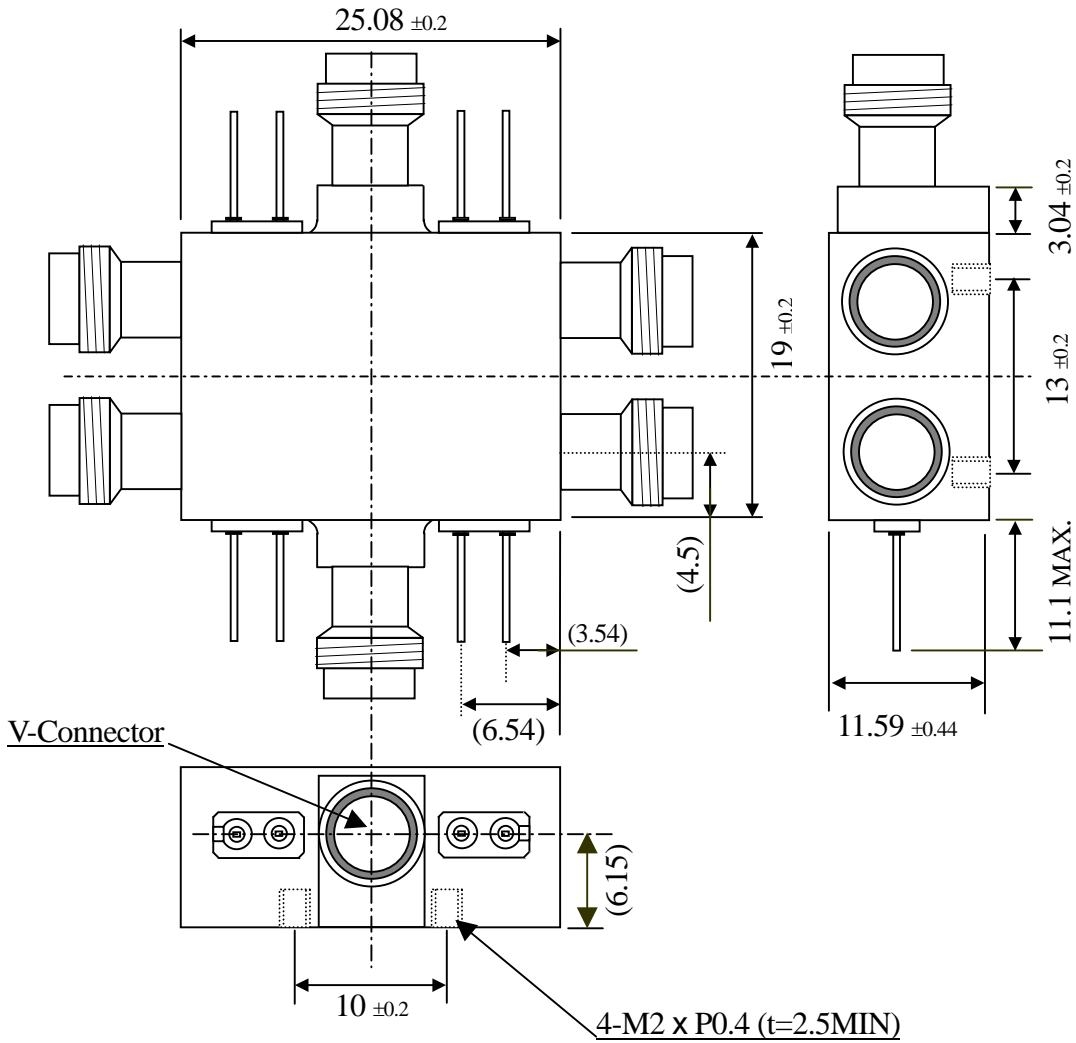
## Power Supply Sequence

- (1) When  $V_{ss}$  is OFF, do not keep the clock input applied to the CKin port for a certain length of time. (Approximately for over 1min.)
- (2) When  $V_{ss}$  is ON, do not keep the device under the condition that the outputs are showing constant high or low level for a certain length of time. (Approximately for over 10min.)

### Note

Use power supplies that do not generate over-voltages such as spikes. Many power supplies generate over-voltages when their outputs are turned on or turned off. To avoid these over-voltages, connect power supplies to  $V_{ss}$  after the power supply outputs are turned on and set to 0 V. Disconnect power supplies from  $V_{ss}$  after the power supply outputs are set to 0 V but before the outputs are turned off.

**SCMD Package Dimension (mm)**



## **Handling Instructions**

Since the IC is fabricated using InP HEMT process, users are recommended to follow the instructions below to prevent damage to the chip from electro-static discharge.

- 1) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
- 2) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M-ohm resistor.
- 3) Ground all test equipment.
- 4) Ground all soldering iron tips.
- 5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

## Caution

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